REMARKS

Claims 1, 2, 4, 5 and 11-16 are pending in this application. Claim 3 is canceled. Claims 6-10, 17 and 18 are withdrawn from consideration. Claims 1, 2, 4, 5 and 11-16 are rejected.

Claim 1 has been amended such that it includes the features of canceled claim 3. Claim 11 has been amended to more particularly point out and distinctly claim applicants' invention. Claim 16 has been amended to correct a typographical error. No new matter is added. The features present in the claims as amended were present in the originally filed specification.

Interview

Applicants are grateful for the time spent by Examiner Douglas Owens in the telephone interview of January 30, 2004 discussing the patent application. During the interview, applicants discussed the proposed amendments to claims 1 and 11 which are amended as set forth above. Applicants also discussed with the Examiner the rejections of the claims by U.S. Patent 6,335,565 to Miyamoto reference as applied in the Office Action. Portions of the arguments put forth by applicant's attorney at the interview are reproduced below.

The Invention as set forth in Claims 1, 2, 4 and 5

The present invention as set forth in amended Claim 1 upon which claims 2-5 depend is directed to a multi-layered semiconductor device which comprises:

1) a film-like semiconductor package 10 an embodiment of which is shown in Figs. 2(a), 2(c), 2(e) and 2(f), for example, which incorporates therein a semiconductor chip 12; and

2) a circuit pattern layer having a package accommodation opening 11c as shown in Figs. 2(b), 2(d) and 2(g). As can be seen in Fig. 2(b) and 2(d), the connecting layer 17 or circuit pattern layer as recited in the claims comprises a substrate 11 and a circuit pattern 13 formed on the substrate 11.

The semiconductor package is accommodated in the package accommodation opening of the circuit pattern layer and thusly constitutes a circuit board. It should be noted that the semiconductor package 10 and connecting layer 17 or circuit pattern layer can be separately made. Then, the semiconductor package 10 shown in Figs. 2(a) and 2(c) is accommodated in the opening 11c of the circuit pattern layer as shown in Figs. 2(b) and 2(d) to form a circuit board. Finally, a plurality of the so formed circuit boards are layered together to form a multi-layer semiconductor device in such a manner that the circuit patterns of the respective circuit boards are electrically connected with each other by means of the low-melting point metal filled in a through-hole.

Thus, a small and thin-sized multi-layered semiconductor device, such as a multi-chip module, incorporating therein a number of semiconductor chips, can be obtained. In particular, according to this invention, the semiconductor chip is not directly in the circuit pattern layer, but is incorporated in the semiconductor package at the package accommodation opening of the circuit pattern layer. Therefore, a laminating or layering operation can be effectively carried out and the semiconductor chip can also be protected by the semiconductor package, resulting in an improvement in the reliability of the multi-layered semiconductor device.

In the invention as set forth in claim 1, the semiconductor packages are not simply layered upon one another, but a combination of structures of the semiconductor packages and the circuit pattern layers are layered with respect to one another. This is in stark contrast to the stacked or layered semiconductor packages of Figs 34 and 35 of Miyamoto.

Thus, with the present invention, a complicated electrical connection can be attained between the respective semiconductor packages. A multi-layered semiconductor device is produced which has a number of semiconductor chips. The resulting semiconductor device can also have a relatively complicated wiring or circuit structure. As a result of the present invention, greater efficiencies and yields can be obtained as compared to previous semiconductor devices.

One advantage that the present invention offers is that one can test or individually check the chips before they are incorporated into the semiconductor package thereby saving the time, effort and expense which occurs in the event that a particular semiconductor chip is found to be defective.

The Rejection of Claims 1-5 under 35 U.S.C. 102(b)

In paragraph 3 of page 2 of the Office Action, the Examiner rejected Claims 1, 2, 4, and 5 under 35 U.S.C. 102 as allegedly being anticipated by Miyamoto. Applicants hereby traverse the rejection of the claims.

The Office Action states that Miyamoto discloses a multi-layered semiconductor device wherein a semiconductor package incorporates a semiconductor chip to form a circuit board. The Office Action then states that Miyamoto teaches in Fig. 34 citing col. 27, lines 5-15, a film-like package incorporating a semiconductor chip and a circuit pattern layer comprising a substrate and a circuit pattern formed on the substrate. It is submitted that the cited portions of Miyamoto do not disclose the invention of the present application but are directed to merely a plurality of packages, each incorporating a semiconductor chip or element which are merely stacked together in an upward and downward directions. This is set forth clearly in col. 6, lines 4-11 of the reference. It is submitted that the cited

portions of the reference suggest nothing about a structure directed to a circuit layer having a package accommodating opening.

In other words, according to the present invention as defined in amended claim 1, the semiconductor packages are not simply layered but the combined structures of the semiconductor packages and the circuit pattern layers are layered with respect to one another which is how applicants invention forms a semiconductor device which provides for complicated electrical connections.

On page 3 of the Office Action and on page 5 of the Office Action, in response to applicants argument in the response of June 13, 2003, the Examiner states that the circuit pattern layer of the opening for the chip is an inherent feature of the device. However, applicants submit that Miyamoto does not even teach the claimed circuit pattern layer for accommodating the structure of a semiconductor package. The semiconductor package 10 as seen in Fig. 2(a) of the present application fits into the package accommodation opening 11c of the circuit pattern layer an embodiment of which is shown in Fig. 2(c), thereby accommodating the semiconductor device. As was discussed with the Examiner during the interview, the semiconductor package of the present invention fits into the package accommodation opening of the circuit pattern layer which is dimensioned and configured to accept or accommodate the semiconductor package. The alleged semiconductor package of Miyamoto does not teach any such structure where the claimed structure of a semiconductor package can be so accommodated. There is no similar structure in the cited reference in which Miyamoto's chip can be fit into. The chips in Miyamoto are merely stacked in an upward and downward direction. (See col. 6, lines 5-15).

As it is respectfully submitted that U.S. Patent 6,335,565 to Miyamoto fails to teach at least one claimed feature of the invention of claim 1, applicants respectfully request reconsideration of the 35 U.S.C. 102 rejection of Claims 1, 2, 4 and 5.

The Invention of Claims 11-16

The multi-layered semiconductor device defined by claim 11 is set forth as follows.

1) a plurality of circuit boards are layered together, wherein each circuit board comprises an insulation substrate, a semiconductor chip incorporated in the substrate, and a circuit formed on a surface of the substrate and electrically connected to the semiconductor chip, and

2) a lead extending from the circuit on the circuit board is bonded, through a through-hole provided in the insulation substrate of the circuit board to a circuit on another circuit board disposed beneath the former circuit board to establish an interlayer connection.

Thus, according to the structure as defined by claim 11, a small and thin-sized semiconductor device, such as a multi-chip module, incorporating therein a number of semiconductor chips, can be obtained.

The Rejection of Claims 11-13, 15 and 16

The Examiner has rejected Claims 11-13, 15 and 16 as being anticipated by U.S. Patent No. 6,335,565 to Miyamoto. Applicants hereby traverse the rejection of the claims 11-13, 15 and 16.

It is respectfully submitted that the portions of the Miyamoto reference cited by the Examiner do not teach the invention of claim 11 nor the claims which depend therefrom.

In response to the Response to applicants arguments of June 13, 2003 on the bottom of page 6 of the Office Action, it is applicants position that Miyamoto only discloses a plurality of semiconductor packages, each incorporating a semiconductor chip or element forming a multi-layered semiconductor device, but does not suggest nor teach the particular claimed connecting structure of leads. With respect to independent claim 11, a typical embodiment of which is shown in Fig. 5, this feature is described on page 11, lines 28-30 as extension 13b which extends into an upper region of through-hole 11d in Fig. 5 from one circuit board to another circuit board below the first circuit board. Applicants submit in response to the Examiner's response to applicants arguments that these features of a lead extending through a through hole in such a manner is not taught in Miyamoto in Fig. 35 and the portion of the text thereof cited in the Office Action.

Accordingly, it requested that the 35 U.S.C. 102 rejection must be withdrawn.

The Rejection of Claim 14 under 35 U.S.C. 103(a)

The Examiner has rejected Claim 14 which is dependent from claim 11 as allegedly being obvious over U.S. Patent No. 6,335,565 to Miyamoto in view of Clark, U.S. Patent 3,672,034. Applicants hereby traverse the rejection of the claim.

It is respectfully submitted that the proffered combination of references cannot render the rejected claims obvious because the secondary Clark reference does not provide the teaching noted above with respect to the above-described features which are absent from the primary Miyamoto reference. Clark is cited in the Office Action for the purposes of showing a disclosure of beam lead bonding for electrically connecting a chip to a circuit board. However, there is no suggestion in Clark of a lead extending from the circuit on the circuit board, that is bonded, through a through-hole of the insulation substrate of the circuit board, to a circuit on another circuit board to establish an interlayer connection.

It is also submitted that Clark suggests nothing about a structure of a multi-layered semiconductor device incorporating therein a semiconductor chip. In fact, Clark suggests nothing regarding an electrical connection between circuit boards which are layered.

Thus, the combination of the cited references fails to teach or suggest all the claim limitations.

Based on the reasoning stated above, Applicant believes one of ordinary skill in the art would not arrive at the present invention by combining Miyamoto with Clark. Therefore, reconsideration of the rejection of Claim 14 and its allowance is respectfully requested.

CONCLUSION

For the reasons set forth above, Applicants' present invention, as recited in the amended claims now more clearly and particularly, is patentable. Reconsideration and withdrawal of all outstanding rejections in this case is hereby respectfully requested.

If further matters remain in connection with this case, the Examiner is invited to telephone the Applicant's undersigned representative to resolve them.

Respectfully submitted,

January 30, 2004

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Order No. 2044